REMARKS

No claims are amended, no claims are canceled, and no claims are added; as a result, claims 1-16 are now pending in this application.

§103 Rejection of the Claims

Claims 1, 4-6, and 10-11

Claims 1, 4-6, and 10-11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Natu (U.S.5,790,850) in view of Hrustich et al. (U.S. 4,639,856). Applicant respectfully traverses the rejection of claims 1, 4-6, and 10-11.

Claims 1, 4-6, and 10-11 are not obvious in view of the proposed combination of Natu and Hrustich et al. because the proposed combination fails to disclose or suggest each of the elements included in claims 1, 4-6, and 10-11.

The Office Action fails to show how the proposed combination of Natu and Hrustich et al. discloses or suggests each of the elements included in claims 1, 4-6, and 10-11. For example, claim 1 recites,

> **designating one processor as a bootstrap processor**;
> testing the bootstrap processor to verify that it will run BIOS code;
> **setting a latch for disabling said bootstrap processor** if the testing indicates a failure. (Emphasis added).

The Office Action on page 3 states, "However, Natu fails to teach setting a latch for disabling the failed bootstrap processor if the testing indicates failure." The Office Action relies on the additional document of Hrustich et al., at column 1, lines 48-53, as disclosing these elements. The relied upon portion of Hrustich et al. states,

> The service processor 11 sets a pair of latches disposed within a failing processor of the multiprocessor computer system. One latch generates an output signal which disables the failing processor. The other latch generates a "miss" signal energizing the remaining processors.

However, there is no disclosure in Hrustich et al. that any of the processors described in Hrustich et al. are designated as a "bootstrap processor," as recited in claim 1. Instead and in contrast, Hrustich et al. discloses,

> If the service processor 11 indicates that the first processor 10 or the second processor 14 is inoperative, the apparatus 30, disposed within the first processor and the second processor, generates an output (trap) signal disabling the inoperative processor, that is, either processor 10 or processor 14. The apparatus 30 includes a latch circuit 30a connected, at one input, to the service processor 11.[1]

Thus, Hrustich et al. discloses that the service processor indicates that a first processor or a second processor is inoperative, but fails to disclose or suggest "designating one processor as a bootstrap processor " and "setting a latch for disabling said bootstrap processor if the testing indicates a failure," as recited in claim 1. (Emphasis added).

Further, there is no disclosure or suggestion in Hrustich et al. that the testing of the processors in Hrustich et al. involves "testing the bootstrap processor to verify that it will run BIOS code," as recited in claim 1. In contrast, Hrustich et al. discloses,

> In a multiprocessor computer system, such as that which is disclosed in British Patent Specification No. 1,163,859 published Sept. 10, 1969, **two or more processors are utilized for the execution of instructions stored in a main memory**.[2] (Emphasis added).

Thus, Hrustich et al. discloses processors utilized for the execution of instructions stored in a main memory, but fails to disclose "testing the bootstrap processor to verify that it will run BIOS code," as recited in claim 1, and thus cannot disclose or suggest, "setting a latch for disabling said bootstrap processor if the testing indicates a failure," as recited in claim 1.

Therefore, the Office Action fails to show how the proposed combination of Natu and Hrustich et al. discloses or suggests each of the elements included in claim 1.

In another example where the proposed combination of Natu and Hrustich et al. fails to disclose or suggest each of the elements included in the claims, claim 6 recites,

> a first processor designated as a bootstrap processor;

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[1] See Hrustich et al. at column 3, lines 55-62.
[2] *See* Hrustich et al. at column 1, lines 14-18.

a latch for turning off said bootstrap processor.

For reasons analogous to those stated above with respect to claim 1, the proposed combination of Natu and Hrustich et al. fails to disclose or suggest "a first processor designated as a bootstrap processor; a latch for turning off said bootstrap processor," as recited in claim 6. Thus the Office Action fails to show how the proposed combination of Natu and Hrustich et al. teaches or suggests each of the elements included in claim 6.

Claims 4-5 depend from claim 1, and so include each of the elements recited in claim 1. Claims 10-11 depend from claim 6, and so include each of the elements recited in claim 6. Therefore, the Office Action fails to show how the proposed combination of Natu and Hrustich et al. discloses or suggests each of the elements included in claims 4-5 and in claims 10-11.

Because, the Office Action fails to show how the proposed combination of Natu and Hrustich et al. discloses or suggests each of the elements included in claims 1, 4-6, and 10-11, the Office Action fails to state a *prima facie* case of obviousness with respect to claims 1, 4-6, and 10-11.

The Office Action fails show some suggestion or incentive to combine the teachings of Natu with Hrustich et al. based on what the combined teaching of Natu and Hrustich et al. would have suggested to those of ordinary skill in the art, and thus fails to meet the requirements for forming the proposed combination of Natu and Hrustich et al.

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). To do that the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would lead an individual to combine the relevant teaching of the references. *Id.*

The *Fine* court stated that:

> Obviousness is tested by "what the combined teaching of the references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 878 (CCPA 1981)). But it "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." *ACS Hosp. Sys.*, 732 F.2d at 1577, 221 USPQ at 933. And "teachings of references can be combined *only* if there is some suggestion or incentive to do so." *Id.* (emphasis in original).

The M.P.E.P. adopts this line of reasoning, stating that:

> In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir. 1991)).

In an attempt to meet these requirements, the Office Action on page 3 states,

> It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Natu to include setting a latch for disabling bootstrap processor if the testing indicates failure, because if the failing processor has internal failure, it may not be able to operate properly to remove itself from the operation. Thus disabling the failing processor eliminates the problem of relying on a failing processor to perform the appropriate action to remove itself from operation.

However, the Office Action fails to point out any portion of the disclosure in either Natu or Hrustich et al. to support these statements. In addition, the statements are contradicted by the very disclosure of Natu. For example, Natu discloses, "The present invention takes advantage of a feature present in some processors that allows the designated BSP to be changed by setting a bootstrap bit and generating a software reset of the computer system."[3] Thus, Natu discloses that the designated BSP may be changed by setting a bootstrap bit and generating a software reset of the computer system. Further, Natu also discloses,

> If the BSP processor is bad or has failed the BIST, the POST goes to step 150 and attempts to reassign the BSP designation to another processor. A BSP is considered to have failed if the BIST has failed for that processor during the current boot, or any previous boot. Any BIST failure is reflected in the status flag.
>
> Step 150 begins a loop in which the BSP will attempt to transfer the BSP designation to each AP until it is successful. At step 150, the BSP determines whether it has attempted to transfer the BSP designation to all

[3] *See* Natu at column 3, lines 23-26.

> of the APs in the system. If it has, at step 165 the initialization has failed because no APs can function as the BSP. The appropriate message is displayed for the user.[4]

Thus, Natu disclose that even when the BSP processor *is bad or has failed*, the POST will attempt to reassign the BSP designation to another processor. Therefore, the disclosure of Natu contradicts the statements made in the Office Action suggesting that a failing processor "may not be able to operate properly to remove itself from operation," wherein as noted above, Natu discloses that a bad or failed processor does in fact attempt to transfer the BSP designation to another processor. Thus, the statements made in the Office Action in support of making the proposed combination of Natu and Hrustich et al. are contradicted by the disclosure of Natu.

Because the statements made in the Office Action in support of forming the proposed combination of Natu and Hrustich et al. are contradicted by the disclosure in Natu, the Office Action fails to provide some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art that would lead an individual to combine the relevant teachings of Natu and Hrustich et al. based on what the combined teaching of Natu and Hrustich et al. would have suggested to those of ordinary skill in the art. By failing to meet these requirements, the Office Action fails to state a *prima facie* case of obviousness with respect to claims 1, 4-6, and 10-11.

For at least the reasons stated above, the 35 U.S.C. § 103 rejection of claims 1, 4-6, and 10-11 cannot stand. Applicant respectfully requests withdrawal of the rejection, and reconsideration and allowance of claims 1, 4-6, and 10-11.

Claims 2-3, 7-9, and 12-16

Claims 2-3, 7-9, and 12-16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Natu (U.S.5,790,850) in view of Hrustich et al. (U.S. 4,639,856) and further in view of Steiert et al. (U.S. 6,122,735). Applicant respectfully traverses the rejection of claims 2-3, 7-9, and 12-16.

[4] *See* Natu at column 3, line 60 through column 4, line 5.

Claims 2-3, 7-9, and 12-16 are not obvious in view of the proposed combination of Natu, Hrustich et al., and Steiert et al. because the proposed combination fails to disclose or suggest each of the elements included in claims 2-3, 7-9, and 12-16.

The Office Action fails to show how the proposed combination of Natu, Hrustich et al., and Steiert et al. discloses or suggests each of the elements included in claims 2-3, 7-9, and 12-16. For example, claims 2-3 depend from claim 1, and so include all of the elements recited in claim 1, and claims 7-9 depend from claim 6, and so include all of the elements recited in claim 6.

Applicant believes they have established that Natu and Hrustich et al., either alone or in combination, fail to disclose or suggest each of the elements included in claim 1 and in claim 6, and therefore fail to disclose or suggest each of the elements included in claims 2-3 and 7-9.

Further, there is no disclosure or suggestion in the additional document of Steiert et al. of the elements included in claims 2-3 and 7-9 and missing from both Natu and Hrustich et al. For example, there is no disclosure or suggestion in Steiert et al. of "designating one processor as a bootstrap processor; testing the bootstrap processor to verify that it will run BIOS code; setting a latch for disabling said bootstrap processor if the testing indicates a failure," as recited in claim 1, and no disclosure or suggestion in Steiert et al. of "a first processor designated as a bootstrap processor; a latch for turning off said bootstrap processor," as recited in claim 6.

In contrast, Steiert et al. discloses,

> When the system is turned on, all processors are enabled at 410. If the system boots correctly at 420, nothing further needs to be done and the system will be fully operational.
>
> If the system does not boot correctly with all processors enabled, one processor at a time is disabled and the start-up process is retried at 430.[5]

Thus, Steiert et al. discloses that when the system is turned on, *all processors* are enabled. However, there is no disclosure in Steiert et al. of "designating one processor as a bootstrap process," and therefore there is no disclosure or suggestion in Steiert et al. of "setting a latch for disabling said bootstrap processor," as recited in claim 1. Also, there is no disclosure in Steiert et al of "a latch for turning off said bootstrap processor," as recite in claim 6.

[5] *See* Steiert et al. at column 2, lines 41-47.

For at least the reasons stated above, the proposed combination of Natu, Hrustich et al., and Steiert et al. fails to disclose or suggest each of the elements included in claims 2-3 and in claims 7-9.

In another example wherein the proposed combination of Natu, Hrustich et al., and Steiert et al. fails to disclose or suggest each of the elements included in the claims, claim 12 recites,

> a timer;
> a latch for turning said bootstrap processor off;
> said timer providing a signal indicating that a predetermined time has expired, **which is applied to said latch to set said latch**. (Emphasis added).

For reasons analogous to those stated above with regards to claims 2-3 and 7-9, the proposed combination of Natu, Hrustich et al., and Steiert et al. fails to disclose or suggest for example, "a latch for turning said bootstrap processor off," as recited in claim 12.

Further, the Office Action on page 3 states, ". . . both Natu and Hrustich fail to teach a timer which indicates a failure if it is not within a predetermined time period." The Office Action relies on Steiert et al. as disclosing these elements, citing timer 300 in Fig. 2 of Steiert et al. However, claim 12 recites that "said timer providing a signal indicting that a predetermined timer has expired, which is applied to said latch to set said latch." The Office Action fails to point out in, and Applicant's representatives fail to find in Steiert et al., a disclosure or suggestion of these elements as recited in claim 12.

Thus, the Office Action fails to show how the proposed combination of Natu, Hrustich et al., and Steiert et al. discloses or suggests each of the elements included in claim 12.

Claims 13-16 depend from claim 12, and so include all of the elements recited in claim 12. Therefore, the Office Action fails to show how the proposed combination of Natu, Hrustich et al., and Steiert et al. discloses or suggests each of the elements included in claims 13-16.

Because, the Office Action fails to show how the proposed combination of Natu, Hrustich et al., and Steiert et al. discloses or suggests each of the elements included in claims 2-3, 7-9, and 12-16, the Office Action fails to state a *prima facie* case of obviousness with respect to claims 2-3, 7-9, and 12-16.

The Office Action fails show some suggestion or incentive to combine the teachings of Natu, Hrustich et al., and Steiert et al. based on what the combined teaching of Natu, Hrustich et al., and Steiert et al. would have suggested to those of ordinary skill in the art, and thus fails to meet the requirements for forming the proposed combination of Natu, Hrustich et al., and Steiert et al.

Applicant believes that for at least the reasons stated above with respect to claims 1, 4-6, and 10-11, the Office Action fails to provide a proper basis for forming the proposed combination of Natu and Hrustich et al. Since the Office Action fails to provide any addition basis for combining Natu and Hrustich et al, in forming the proposed combination of Natu, Hrustich et al., and Steiert el al. in rejecting claims 2-3, 7-9, and 12-16, the Office Action also fails to state a *prima facie* case of obviousness with respect to the rejection of claims 2-3, 7-9, and 12-16.

In addition, in an attempt to meet the requirements for forming the proposed combination of Natu, Hrustich et al., and Steiert et al., the Office Action on pages 3-4 states,

> It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Natu to include a timer which indicates a failure if its is not reset within a predetermined time period, because it gives the BSP a chance to initialize and begin normal operation [*see Steiert, col. 3, lines 5-11*]. (Emphasis in original).

However and in contrast, Natu discloses,

> In the present invention, the designated BSP determines it has failed after examining its corresponding status bits. The BSP is determined to have failed if its status bits reflect that it has failed during the current boot, or any previous boot.[6]

Thus, Natu relies on examination of a status bit to determine if the BSP has failed, and so would not require a timer, as suggested by the Office Action, to indicate a failure.

Because the statements made in the Office Action in support of forming the proposed combination of Natu and Steiert et al. are contradicted by the disclosure in Natu, the Office Action fails to provide some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art that would lead an individual to combine the relevant teachings of Natu and Steiert et al. based on what the combined teaching of Natu and Steiert et

[6] *See* Natu at column 2, lines 63-64.

al. would have suggested to those of ordinary skill in the art. By failing to meet these requirements, the Office Action fails to state a *prima facie* case of obviousness with respect to claims 2-3, 7-9, and 12-16.

For at least the reasons stated above, the 35 U.S.C. § 103 rejection of claims 2-3, 7-9, and 12-16 cannot stand. Applicant respectfully requests withdrawal of the rejection, and reconsideration and allowance of claims 2-3, 7-9, and 12-16

Reservation of Rights

Applicant does not admit that references cited under 35 U.S.C. §§ 102(a), 102(e), 103/102(a), or 103/102(e) are prior art, and reserves the right to swear behind them at a later date. Arguments presented to distinguish such references should not be construed as admissions that the references are prior art.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 371-2132) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 14 day of June, 2006.

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